PHASE-ADJUSTMENT OF DIVIDED CLOCK IN DISK HEAD READ CIRCUIT

This application claims the benefit under 35 U.S.C. § 1.119(e) of a provisional application filed July 11, 2000, entitled "Race Avoidance In Disk Head Read Circuit", Application No. 60/217612, the contents of which are incorporated by reference.

This application is a continuation of Application Serial No. 09/660,929, filed on September 13, 2000, the contents of which are incorporated by reference.

BACKGROUND OF THE INVENTION

Field Of The Invention

The present invention relates to read circuitry for a disk head, and in particular relates to phase-adjustment of a divided clock in such a read circuit, so as to avoid race conditions between time of data validity and latching of such data in accordance with the divided clock.

Description Of The Related Art

Read circuits for a disk head provide an interface between a magnetic disk head and a hard disk controller, so as to provide verified digital parallel data to the hard disk controller. Such read circuits include a time base generator phase-locked to the output of the disk head so as to provide a high frequency clock reference, together with a divider to provide a divided clock signal for use in latching digital data. A generalized block diagram for a conventional read circuit, showing the time base generator and the divider, is shown in Figure 1.

As shown in Figure 1, read circuit 1 accepts as input the pre-amp output from pre-amp 2 which amplifies the analog output from disk head 3. Read circuit 1 provides 9-bit digital data 4 to hard disk controller 5, which in turn provides the digital data to computer bus 6. Internally, read circuit 1 includes a time base generator 8 phase-locked to the output of pre-amp 2 so as to provide a high frequency clock signal 9. In addition, divider 10 operates to divide the output from time base generator 8 (such as division by 8, 8½, or 9) so as to provide a divided clock signal 11. A/D converter 12 converts the analog output from pre-amp 2 into a digital output such as a 6-bit digital output which is provided to detector 14 (such as a Virterbi detector) which outputs a 1-bit digital signal which is a verified digital bit corresponding to the bit stored on the hard disk. A sequence of such 1-bit digital signals is provided to serial-to-parallel data formatter 15, which converts the 1-bit digital serial data into 9-bit parallel data which includes a parity bit. Each of A/D converter 12, detector 14 and data

formatter 15 operate in accordance with high frequency clock 9.

The 9-bit parallel data from data formatter 15, shown at reference numeral 16, is provided to latch 17 which latches the data at a timing determined by divided clock 11. The latched parallel data is thereafter provided to hard disk controller 5, as described before.

Figure 2 is a timing diagram showing the timing of some signals in the Figure 1 block diagram. (a) is high frequency clock 9, (b) is the 6-bit output of A/D converter 12, (c) is divided clock 11, and (d) shows validity of 9-bit data 16. As shown in Figure 2, high frequency clock 9, such as a 600 mHz clock, is divided by divider 10 (in this example, a divide-by-eight divider) into divided clock 11. Superimposed on the waveform for divided clock 11 are count numbers showing the count by which divided clock 11 is created.

Superimposed on A/D converter output 13 is a well-known synchronization marker 20 (hereinafter "SM"), which follows the equally well-known synchronization field. Upon encountering the synchronization marker, digital data from the disk head immediately follows. Digital data here is indicated by numerals 21, also superimposed on the A/D converter output 13, which indicate the bit number of the data. 9-bit data 16 is valid after eight bits of data have been collected from the disk head and the ninth parity bit has been added by formatter 15, as shown in Figure 2.

Because of the construction of conventional read circuits, it is possible for a race condition to

arise between the timing at which data 16 is valid and the timing when latch 17 latches the data in accordance with the rising edge of divided clock 11. This race condition is depicted at 22 in Figure 2, and arises primarily for two reasons. First, because time base generator 8 is phase-controlled to lock with data from the disk head, its phase moves, causing a corresponding movement in phase of divided clock 11. Second, because the occurrence of the synchronization field and the synchronization marker is asynchronous with operation of divider 11, divider 11 is never exactly certain of where, in the output of high frequency clock 9, 9-bit data 16 will be valid.

SUMMARY OF THE INVENTION

It is an object of the invention to address the foregoing situation, through the provision of a divider whose phase is adjustable in response to detection of the synchronization marker.

In one aspect, the invention is a read circuit which provides multi-bit disk data to a disk controller based on analog data from a disk head. The read circuit includes a high frequency clock, a bit detector synchronized by the high frequency clock to provide single-bit verified digital data corresponding to the analog output of the disk head, a serial-to-parallel data formatter for formatting the single-bit data into parallel data, and a synchronization mark detector for detecting a synchronization mark. The synchronization mark detector can be arranged to detect the synchronization mark based on the single-bit data

from the bit detector. A clock generator generates a lower frequency clock from the high frequency clock, such as by dividing the high frequency clock, with the phase of the clock generator being adjustable in response to the synchronization mark detector. A latch operating in response to the adjusted lower frequency clock latches the parallel output from the serial-to-parallel converter, for use by the disk controller.

Preferably, the high frequency clock is phase-locked to the output of the disk head, and further provides synchronization for an A/D converter that provides digital data to the bit detector. In particularly preferred forms, the clock generator, which generates the lower-frequency clock, operates by a reset of a counter which counts the number of pulses from the high frequence clock. The reset is responsive to the synchronization mark detector so as to reset the counter in a situation where a race condition might arise, and so as not to reset the counter in a situation where a race condition surely would not arise.

Because the phase of the clock generator is adjustable in response to a synchronization mark detector, it is possible to adjust the phase such that a race condition with the timing of valid data does not arise.

This brief summary has been provided so that the nature of the invention may be understood quickly. A more complete understanding of the invention can be obtained by reference to the following detailed description of the preferred embodiment thereof in connection with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing a conventional read circuit, and Figure 2 is a timing diagram for the Figure 1 block diagram.

Figure 3 is a block diagram of a read circuit in accordance with an embodiment of the invention, and Figure 4 is a timing diagram showing three different examples of phase adjustment for the block diagram of Figure 3.

Figure 5 is a block diagram showing reset circuitry for providing a clock generator whose phase is adjustable in response to a synchronization mark detection.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 3 is a block diagram of a representative embodiment of the invention, in which phase of a lower-frequency clock generator is adjusted in accordance with detection of the synchronization marker.

Figure 3 shows read circuit 100 which accepts analog output from pre-amp 102 whose input is an analog signal from a disk head 103. Read circuit 100 converts the analog signal from pre-amp 102 into 9-bit digital parallel data 104 and provides the 9-bit data 104 to hard disk controller 105 which, in turn, outputs the digital data to computer bus 106.

Internally of read circuit 100, a time base generator 108 phase-locked to the analog output of pre-

amp 102 generates high frequency clock 109. A clock generator 110 provides a divided clock output 111, such as division by 8, 8½, or 9, from high frequency clock 109. The phase of divided clock 111 is adjusted in accordance with a detection of the synchronization marker, as described more fully below.

A/D converter 112 converts the analog output from pre-amp 102 into 6-bit data 113 which is provided to single-bit detector 114. Detector 114, which may be a Virterbi detector, generates a verified single-bit output based on the 6-bit data 113, representative of digital data stored on the hard disk. A/D converter 112 and detector 114 operate in synchronism with high frequency clock 109.

A serial-to-parallel data formatter accepts the single-bit output from detector 114 and converts it to parallel 9-bit digital data 116. Data 116 is latched by latch 117 in accordance with the rising edge of divided clock 111 so as to provide 9-bit digital parallel data 104, which is provided to hard disk controller 105 as described before.

Detector 118 detects the synchronization marker in data from the disk head. In this embodiment, detector 118 operates based on the single-bit output from detector 114, so as to provide a SM detection pulse 119. Other arrangements for the detector are possible, such as arrangements in which the synchronization mark is detected based directly on analog data from pre-amp 102 or based on the digital data from A/D converter 112. The SM detection pulse 119 is provided to clock generator 110 so that clock generator 110 can adjust its phase so as to avoid a

race condition with validity of 9-bit data 116. This operation is described more fully below in connection with the timing diagram shown in Figure 4.

Figure 4 is a timing diagram showing the timing relationship between some of the signals in the Figure 3 block diagram. (a) depicts high frequency clock 109 such as a 600 mHz clock, and (b) shows output 113 from A/D converter 112. In a first example of timing, (c) shows SM detection pulse 119 from synchronization marker detector 118, (d) shows divided clock 111 from clock generator 110, and (e) shows 9-bit data 116 from data formatter 115. In a second example of timing, (f), (g) and (h) correspond respectively to SM detection pulse 119, divided clock 111, and data 116; and in a third example of timing (i), (j) and (k) respectively correspond to SM detection pulse 119, divided clock 111 and data 116.

Superimposed over output 113 from A/D converter 112 is synchronization marker 120. Also superimposed over output 113 from A/D converter is the bit number 121 of data contained within the output.

Turning to a first example of timing, superimposed on divided clock 111 is a count showing an internal count from clock generator 110 of high frequency clock 109. As shown at (d), the count is identical to that of Figure 2, and thus would result in a race condition with the timing of validity of data 116. According to the invention, however, phase of the divided clock 111 is adjusted in accordance with the SM detection pulse 119. Specifically, as shown at (d) in Figure 4, SM detection pulse 119 is generated by synchronization marker detector 118 one cycle after its

occurrence at 120. In response to the SM detection pulse, clock generator 110 resets its internal count as shown at 112a. The reset causes the count to begin again, thereby adjusting the phase of divided clock 111 by extending it for one additional clock cycle of high frequency clock 109. As a result of this phase adjustment, data 116 is valid at the rising edge of divided clock 111 resulting in an absence of a race condition, as depicted at 123a.

In this embodiment of the invention, a reset the count is reset any time that SM detection pulse 119 occurs within the first half cycle of divided clock 111, and the count is not reset if the SM detection pulse occurs within the second half cycle of divided clock 111. This is shown in the second example, at (f), (g) and (h). There, SM detection pulse 119 occurs at the second count of high frequency clock 109 in clock generator 110. Accordingly, the internal count is reset as shown at 122b, thereby resulting in the absence of a race condition as shown at 123b.

Because of the reset of the internal count at 122b, the phase of the divided clock is adjusted in accordance with the SM detection pulse so as to avoid a race condition.

In the third example, shown at (i), (j) and (k), no reset occurs because SM detection pulse occurs in the second cycle of divided clock 119. No reset occurs since none is needed to avoid a race condition, as shown at 123c.

Figure 5 is a block diagram showing an internal construction for clock generator 110. As shown in Figure 5, divider 130 provides divided clock

output 111 in accordance with division of a high frequency clock 109. Divider 130 typically divides by 8, 8½ or 9. Divider 130 further includes a reset terminal which resets its division in accordance with the output of cycle counter 131. Cycle counter 131 monitors the current cycle count of high frequency clock 109, so as to determine whether divider 130 is operating in its first half or second half cycle. Upon occurrence of SM detection pulse 118, if cycle counter 131 determines that divider 130 is operating in its first half cycle, it issues a reset pulse so as to adjust the phase of divided clock 111. Conversely, if cycle counter 131 determines that divider 130 is operating in the second half cycle, no reset pulse is issued upon receipt of the SM detection pulse 118.

The invention has been described with respect to particular illustrative embodiments. It is to be understood that the invention is not limited to the above-described embodiments and that various changes and modifications may be made by those of ordinary skill in the art without departing from the spirit and scope of the invention.